Beyond 3D. Manufacturing process development requirements for multi material wafer scale packaging

John Sweet, Loadpoint Ltd., Cricklade, SN6 6HE UK, john.sweet@loadpoint.co.uk

Multi layer wafer scale packaging is becoming attractive as wafers get bigger and intermediate package costs, such as BGA, μBGA and QFN, increase. Consideration now has to be given the key parameters for dicing, grinding and other associated processes that will be required as the wafer scale packaging process moves beyond pure silicon structures to components that include sensors and actuators, typically in the form of MEMS and PZT devices. Key manufacturing technologies need to be considered at this point to ensure the development of wafer stacking technology is successful. These include through silicon vias, interposer manufacture, grinding, with CMP and dicing. The types of material in the package may mean major changes or developments in current procedures.

Consideration of the processing and the key techniques together with design for test, manufacturing and quality will be critical for the development of “stacked” technologies when sensors / actuators are integrated with their controllers. The order of the development of the manufacturing process for multiple material stacks will be critical as the material technologies will have very different characteristics and there are critical decisions that have to be taken very early in the development process.

Loadpoint has been involved in the electronics industry since 1963, originally a semiconductor device manufacturer. In this time it has focused on “niche” market opportunities and has always maintained a forward view of the potential development for it’s products. It has a multi facetted view of the industry due it’s involvement in process development, machine supply and air bearing sales. The latter, being to 3rd party process providers, does give a different perspective not normally available to other commentators. These 3 points give Loadpoint a unique perspective on the development of new markets.

Over the past 2 years there has been an increasing amount of information and discussion on 3D packaging for silicon in the industry. This has been driven by several factors and figure 1 is a summary of the situation in the autumn of 2007. The key points from this being via diameter, wafer thickness and number of layers, changing as the manufacturing techniques become more developed over time. What is relevant to this paper is the almost total focus on silicon and the relatively high level of technology that is involved. The silicon 3D work does provide a context for the migration of the stacking technique into new areas of interest.

In a forward looking paper such as this it is necessary to “think freely” without restrictions as this approach might open up manufacturing routes and ideas that could be precluded from a more cautious iterative development approach.

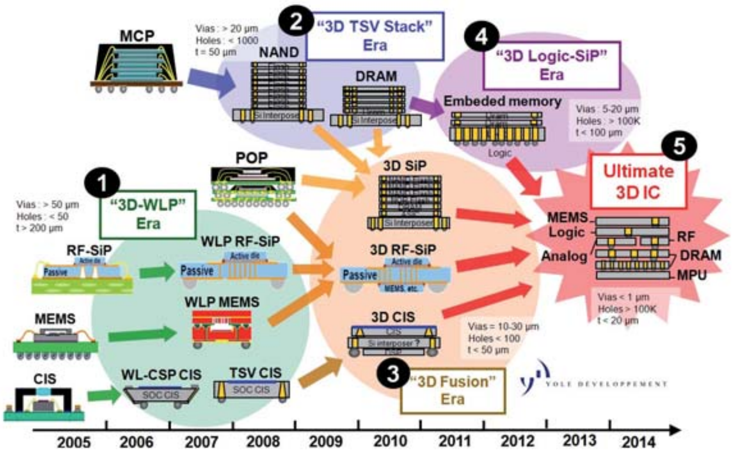
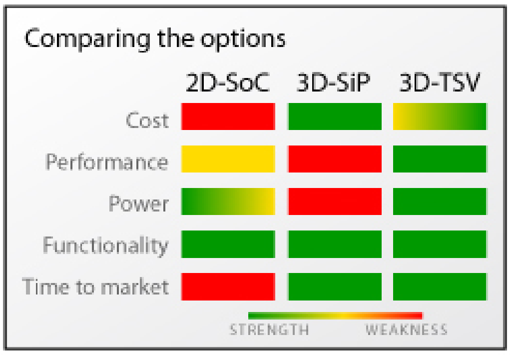


Figure 1,Wafer level packaging evolution 2005 to 2014, courtesy Yole developments

Sematech are a key player in this emerging technology and figure 2 reflects their over view of the current emerging situation. Again it is focussed on silicon however if other materials are considered for the multi material stacks the same advantages may be available. More especially if the technical requirements are not so stringent with respect to placement accuracy and similar points requiring fine process control.



Comparing the options

	2D-SoC	3D-SiP	3D-TSV
Cost	🟥	🟩	🟨🟩
Performance	🟨	🟥	🟩
Power	🟩🟨	🟥	🟩
Functionality	🟩	🟩	🟩
Time to market	🟥	🟩	🟩

STRENGTH WEAKNESS

3D TSVs offer a cost-effective way to achieve high density and performance while also being able to integrate non-CMOS products with CMOS. The SEMATECH project is based on cost modeling to assure products will be manufacturable and affordable.

Figure 2 Sematech comparison chart for silicon CMOS options,

The sophistication of the marketing for wafer scale products means that potential suppliers to the industry have to work very closely with their customers. So key market needs are identified several years ahead of need. The need is now heavily influenced by legislation, as in the USA. So the market can be seen to be actively "pulling" manufacturing processes through the development cycle. This is influenced also by the tight feedback loops in current statistical process control techniques and major manufacturing issues as generally experienced. In some ways the high legislative requirement in the Automobile industry could be seen as a burden however the enhanced safety requirement does cause major changes that can be handled economically through changes in packaging. Environmental aspects are now critical and the features per unit volume concept can also be enhanced by consideration of packaging processes.

Wafer scale or chip on wafer has already been used in the MEMS industry. Both Invensense and SiTime have used this to their advantage. A typical issue is gaining access to boding pads. Some do this by removing a strip over the pads, such as Ivensense and some projection chip manufacturers. Not always an easy technology. Flip chip onto an interposer or spreader is another solution.

Before taking the discussion further the difference as we understand it between wafer scale and frame packaging should be considered. Wafer scale dicing uses the more conventional dicing machine and related technology approach. In many ways it is a simple technology and very flexible. Dicing of frames uses a specific type of machine called a singulator that can be highly single product focussed and so not that flexible. They are very productive and can incorporate device inspection and test in some models. However the wafer scale approach may eliminate several process steps with a reduction in materials going to scrap as part of the process. It would also be much simpler and more suitable for low to medium volume higher margin specialist applications.

Loadpoint has been developing wafer scale package dicing processes since 1978. The first packages were air bag pressures sensors for AC Delco. These consisted of silicon and borosilicate glass wafers 3.3 mm thick. Since then experience has been gained with many other customers and technologies such as IBM Power PC™, Nokia, TI DLP™, VTI and Ya Hsin SMD LEDS.

For wafer scale technology to work there are several critical technologies needed. The Through Silicon Via, TSV, is critical to this as it overcomes the wafer to device lead bonding issue. Via’s can also be used as part of an interposer or spreader technique. In the other techniques needed planarisation is critical not only to ensure flat surfaces for subsequent bonding processes but also to maintain parallelism as the wafer stack is built up. There is an interchange between one to one pad bonding and the use of interposer technology. Multi-way via’s could lead to simplifications.

Wafer scale bonding has been well developed in the MEM’s industry for bonding glass and other materials to silicon. Up to 6 layers have been bonded and the techniques for this are well known. However the introduction of via’s needs to be considered in detail as in most cases isostatic bonding has involved flat single material surfaces.

A critical process in 3D wafer bonding is the thinning of the silicon wafers as the stack is built up. This is normally achieved by etching or grinding with CMP to provide the high surface quality needed for the next bonding operation. Critical to this will be ability of the thinning techniques to handle the metal in the via’s and keeping a planar surface across the dissimilar materials. A technique that will be useful to this will be dicing by grinding. In this the wafer will be partially diced through 25% of it thickness, bonded to the next wafer and then ground back to the required thickness. This will result in very high quality back of wafer” surface quality and cleanly separated die. The grinding process should not be affected by the metal in the via’s, it would be essential that they were filled so no grinding swarf accumulated in the void.

The method for building up the stack will reflect the characteristics of the layers of material. In some instances it would be logical to use the strongest material as a “handle” and build up the layers either on top or below. The structure outlined in figure 3 does reflect concepts that have been part of funding applications in medical ultra-sonics. In this the active PZT layer was at the top as it acts in both receive & transmit mode or sense & actuate mode in a pressure sensitive actuator mode.

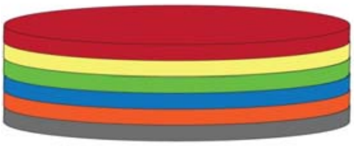
Level	*Material*	*Function*	
1	*PZT*	*Sensor / actuator*	
2	*Ceramic*	*Absorber*	
3	*Silicon*	*Driver*	
4	*Silicon*	*Processor*	
5	*Silicon*	*Interposer*	
6	*PCB*	*Connection*	

Figure 3 Proposed structure for high frequency medical scanner

A theoretical structure would entail both sensors and actuators with structural elements, especially if it was going to be used in a harsh environment. The silicon elements could be interconnected by via’s with the external connection using BGA, µBGA or QFN structures. There might also be the possibility of a hybrid external inter-connect method being developed to handle specific needs, such as ruggedness or operation in extreme environmental conditions. This approach is now part of a €5.2 million research project investigating the manufacture of Acoustic Tweezers by 4 British universities.

In order to determine practically the process steps that should be considered a 6 layer test piece was assembled from samples already available at Loadpoint. This contained a number of key materials and enabled some of the critical manufacturing points to be identified. A key part of this was the glass, silicon, glass, silicon wafer scale module that was already available as an assembly. Figure 4 shows the structure after it had been diced.

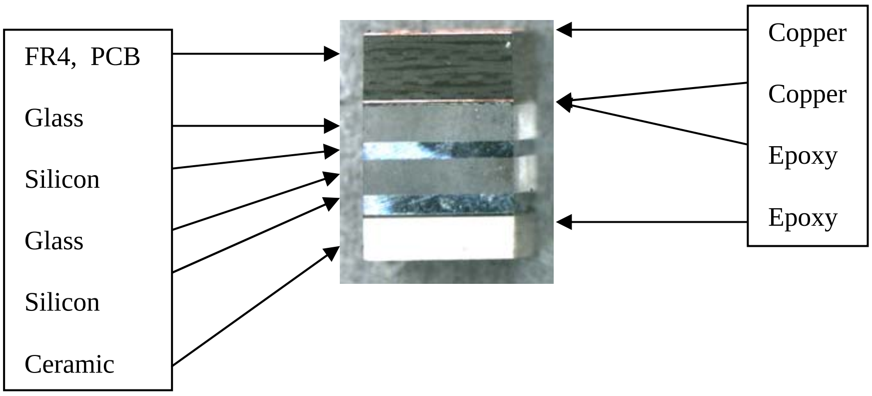


Figure 4 Six layer test piece after dicing

However what is critical is that it is not a 6 layer structure but a 10 layer structure if the intermediate layers on the right hand side are included, being the various bonding and circuit defining layers. It is expected that there will be several layers of filled epoxy in such structures. So the processing of such materials will be critical, fortunately most filled epoxies either grind or dice well and this could be used to advantage. The next logical step is to consider all the processing steps that might be involved. Some might be mutually exclusive or inclusive depending on what is needed.

In this analysis several of the processes are already available. However it is relevant to identify those where more work will be needed as this would be the major part of any project. Figure 5 identifies some of those processes where further work is needed as well as those where there are established sources of knowledge. This would need to be confirmed in the consideration of detailed applications. It is expected that this technology would be highly application orientated and the initial steps would entail defining those steps that are common to most applications to set up a common "tool box" of processes. (This list does need expanding for specific projects).

Process	***Possible sources or development needed***
Routing & drilling FR4.	PCB Industry.
Photo-etching Copper or inter-connect material on non silicon materials.	PCB Industry, thin and thick film hybrid technology.
Ink Jet printing of electrical circuits.	Emerging circuit ink jet printing companies.
Grinding silicon.	Exists already.
CMP silicon.	Exists already.
Planarisation CMP.	Evolution outside silicon needed.
Planarisation, grinding.	Needs to be explored outside silicon.
Grinding & CMP glass.	Optical industry or MEMS.
Grinding of epoxy and ceramic.	Development needed, especially with mixed materials.
Lapping, were suitable.	Exists already, development needed.
Fly cutting.	Rapidly emerging, development needed.
Via's in silicon, glass, FR4 and ceramic.	Silicon evolving, glass development needed, possibly micro-sand blasting. FR4 PCB industry.
Iso-static bonding silicon to glass.	Established bonding organisations.
Bonding processes, not iso-static.	Development needed.
Bulk removal by DRIE of Silicon.	Exists already.
Cavity machining.	Moulding, etching, machining.
Injection of epoxy.	Back fill or under fill from flip chip bonding.
Bumping and under fill.	Exists already in silicon industry.
Dicing of all or sub-elements.	Design of wafers and process critical for this.
Inspection of internal structures.	100% of all by X ray or ultrasonic imaging.

Figure 5 Processes requiring development or existing already.

A wafer stacking technology may require other ideas to handle different needs. These could include internal screening for RF isolation, islands for mounting devices above the plain of the sub layer or cavities for location of discreet devices. Shapes and curves in 2 or 3 D form may be useful and these could be milled or etched into the layer by chemical or mechanical means. Optical circuits might also be added as well as larger sub-elements elements such as "lab on a chip" and such like.

The use of simulations is highlighting many of the issues before actual manufacture. Figure 6 is a simulation of a wafer scale structure that now includes sensor, actuator devices on the top surface with an absorption layer directly underneath. The structure then includes Piezo-electric materials, loaded epoxy, glass, silicon, glass, silicon and ceramic. (Simulations have proved to be very useful in the development of 3D silicon structures both as feasibility and the investigation of manufacturing costs.)

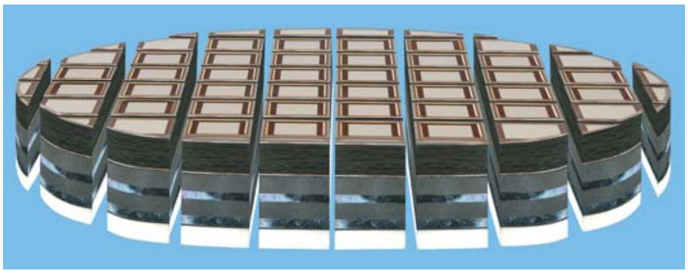


Figure 6 Simulation of Ultrasonic structure

The dicing of the wafer scale structure could use a heavy duty dicer and single or multiple blade dicing machines can be used. Some thick structures using steel or hard metals might need very heavy duty dicing machines. All the dicing blade and work holing techniques would be based on currently available processes, although some might need considerable adaptation.

Stacking of wafers will require consideration of several other key points. Tolerances of the various technologies need to be kept in mind as well as the differences in rates of thermal expansion. This part of the project development has to be very carefully considered from the beginning. Whilst dicing is considered a stable established technology it is expected to generate some major problems. It is therefore important that as many points regarding dicing are considered from the beginning. In fact there are several processes where a "design for" approach could be used. These would include grinding, planarisation, bonding, etching, filling amongst others. Testing and fault finding must also be considered from the beginning in a "design for" approach.

Material sensitivity Street width
Thickness of material
Sensitive surface structures
Static problems
Shape
Edge chipping
Thinning requirements

Figure 7 "Design for" dicing points

This list typifies the points to be considered in a "design for" approach. Some of the combinations of processes are unique and will require considerable thought at this stage. The output of a wafer scale technique would be designed to integrate with a tape and reel process. This approach would enable parts to be automatically bonded into larger elements. (Interestingly the wafer scale technique envisaged would lead to a considerable drop in the part count of any system using this concept)

For the general dicing a Loadpoint NanoAce includes all the critical features that are needed. This would include the ability to handle thick materials, highly flexible programming and a pattern recognition system capable of handling difficult to see fiducials. It is expected that wafer scale assemblies will get thicker. For this very heavy duty machine will be needed. The MacroAce has the necessary capacity and features. Critical to the multi wafer process will be the ability to grind wafers to a high dimension tolerance. The Loadpoint PicoAce has already proven it's capability to handle this type of application. It can also be adapted for fly-cutting as part of the planarisation process. It should be noted that grinding or fly-cutting generates good geometry quickly and CMP then improves the surface finish, when required.

There is a considerable amount of information already on the web. Much of it is very useful and it appears that we are all in an unofficial pre-competitive phase whilst all the key production requirements are being defined. The market seems to be "pulling through" the techniques it requires and the potential suppliers are refining their equipment capabilities to meet that market as well as defining what is available. The cost reductions achievable could be considerable, more especially as the hardware is already developed and it will be the characterisation and process development that will provide the challenges.

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deliberately. Further development would be project specific and the intellectual property could then be accurately defined in a practical way.

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